

IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A computer system comprising:
an authorized user identification device;
at least one processor coupled to the computer system;
a proximity range actuated~~an~~ identification signal detection circuit for
receiving a wireless identification signal from ~~an~~ the identification object device,
the wireless identification signal containing identification information regarding
~~the assigned processor~~ a user of the device ~~identification object;~~
a memory having means for determining whether ~~the assigned processor~~
user of the identification object device as indicated by the wireless identification
signal, has authorized access to computer information accessible by the
computer system; and
a memory having means for placing the computer system in a condition to
deny access by placing the computer system in a lower power state in response
to the identification signal detection circuit not having received, for a
predetermined period of time, a wireless identification signal containing
identification information from ~~an assigned processor~~ the user having authorized
access.
2. (Original) The computer system of claim 1 further comprising:
a memory circuit programmable to store a list of at least one user having
authorized access to computer information assessable by the computer system.
3. (Canceled)
4. (Canceled)

5. (Currently Amended) The computer system of claim 1 wherein placing the computer system in a condition to deny further includes logging a user off of the computer system in response to the identification signal detection circuit not having received for a predetermined period of time, a wireless identification signal containing identification information from ~~an assigned possessor~~ the user having authorized access.
6. (Currently Amended) The computer system of claim 1 wherein placing the computer system in a condition to deny further includes placing the computer system in a locked state in response to the identification signal detection circuit not having received for a predetermined period of time, a wireless identification signal containing identification information from ~~an assigned possessor~~ the user having authorized access.
7. (Currently Amended) The computer system of claim 1 further comprising:
a memory circuit storing operating system code whose execution by the at least one processor implements an operating system for controlling the operation of the computer system; and
wherein the operating system code includes code whose execution places the computer system in a condition to deny access to computer information accessible by the computer system in response to the identification signal detection circuit not having received for a predetermined period of time, a wireless identification signal containing identification information from ~~an assigned possessor~~ the user having authorized access.
8. (Cancelled).

9. (Cancelled).
10. (Currently Amended) The computer system of claim 1 wherein:
the memory having means for determining that the identification signal detection circuit has not received the wireless identification signal for a predetermined period of time is implemented in the identification signal detection circuit; and
the identification signal detection circuit provides a response signal in response to a determination that the identification signal detection circuit has not received for a predetermined period of time, a wireless identification signal containing identification information from ~~an assigned possessor~~ the user having authorized access.
11. (Currently Amended) The computer system of claim 10 wherein the identification signal detection circuit generates an interrupt in response to a determination that the identification signal detection circuit has not received the wireless identification signal for a predetermined period of time.
12. (Currently Amended) The computer system of claim 10 wherein the identification signal detection circuit asserts a #PME signal in response to a determination that the identification signal detection circuit has not received the wireless identification signal for a predetermined period of time.
13. (Original) The computer system of claim 12 further comprising:
a chipset circuit having an input to receive the #PME signal from the identification signal detection circuit.
14. (Currently Amended) The computer system of claim 1 wherein the memory having means for determining whether ~~the assigned possessor~~ user of the

~~security object~~ device and the memory having means for determining that the identification signal detection circuit has not received the wireless identification signal for a predetermined period of time, are both implemented in the same memory circuit of the identification circuit.

15. (Currently Amended) The computer system of claim 1 wherein the identification signal detection circuit is operably coupled to ~~the processor via~~ a power managed computer bus.
16. (Currently Amended) The computer system of claim 1 wherein:
 - the identification signal detection circuit has an output to provide an indication signal indicating that the identification signal detection circuit has received a wireless identification signal containing identification information of ~~an assigned possessor~~ the user of ~~a security object~~ the device determined to have authorized access; and
 - wherein ~~the identification~~ indication signal is provided in response to receiving a wireless identification signal containing identification information of ~~an assigned possessor~~ the user of ~~a security object~~ the device determined to have authorized access after a predetermined period of time of not receiving an identification signal containing identification information of ~~an assigned possessor~~ the user of ~~a security object~~ the device determined to have authorized access.
17. (Original) The computer system of claim 16 wherein:
 - the identification signal detection circuit is operably coupled to the at least one processor via a computer bus substantially conforming to a PCI Local Bus Specification; and
 - the indication signal includes an assertion of the #PME signal.

18. (Currently Amended) The computer system of claim 1 further comprising:
a memory having means for placing the computer system in a higher power state from a lower power state if it is determined that the identification signal detection circuit has received a wireless identification signal containing identification information of ~~an assigned possessor~~ the user having authorized access.
19. (Cancelled).
20. (Cancelled).
21. (Currently Amended) A method for controlling access to computer information comprising:
providing an authorized user identification device;
providing a computer system;
sending a wireless identification signal by ~~an~~ the identification ~~object device~~, the wireless identification signal including identification information regarding ~~an assigned possessor~~ a user of the ~~object device~~;
receiving, independent of a conscious access action by ~~a~~ the user, the wireless identification signal by a proximity range actuated detection circuit coupled to the computer system;
determining whether the ~~assigned possessor~~ user as indicated by the wireless identification signal has authorized access to computer information accessible by ~~a~~ the computer system;
granting access to computer information accessible by the computer system if it is determined that the ~~assigned possessor~~ user as indicated by the wireless identification signal is authorized access, wherein the granting access to computer information accessible by the computer system further includes placing the computer system in a higher power state from a lower power state; and

denying access to computer information accessible by the computer system by placing the computer system in the lower power state if the computer system has not received for a predetermined period of time, a wireless identification signal containing identification information from ~~an assigned possessor~~ the user having authorized access.

22. (Cancelled).

23. (Cancelled).

24. (Cancelled).

25. (Cancelled).

26. (Canceled)

27. (Cancelled).

28. (Cancelled).

29. (Cancelled).

30. (Cancelled).

31. (Cancelled).

32. (Cancelled).

33. (Cancelled).

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34. (Cancelled).

35. (Cancelled).

36. (Cancelled).

37. (Cancelled).